IN THE CLAIMS:

Please consider the following claims:

1. (Currently amended) An electronic circuit, comprising:

a plurality of input/output (I/O) nodes for connecting the electronic circuit to at least a further electronic circuit;

a test unit for testing the electronic circuit in a test mode of the electronic circuit, the test unit comprising a combinatorial circuit having a plurality of inputs and an output, the combinatorial circuit implementing an exclusive logic function;

the I/O nodes being logically connected to the test unit in the test mode, wherein:

a first selection of the I/O nodes is arranged to carry respective input signals and is connected to the plurality of inputs of the combinatorial circuit; and

a second selection of the I/O nodes comprises a first I/O node and is arranged to carry respective output signals, the first I/O node being coupled to the output of the combinatorial circuit; and

the second selection of I/O nodes further comprises a second I/O node that is coupled to an I/O node from the first selection of I/O nodes in the test mode via a connection that includes at least one of a buffer and an inverter, wherein the inverter facilitates a third I/O node from the second selection of I/O nodes being coupled to a further I/O node from the first selection of I/O

nodes via a connection that bypasses the combinatorial circuit, and the buffer facilitates at least the second I/O node being coupled to the I/O node from the first selection of I/O nodes.

2. (Canceled).

3. (Previously presented) An electronic circuit, comprising:

a plurality of input/output (I/O) nodes for connecting the electronic circuit to at least a further electronic circuit;

a test unit for testing the electronic circuit in a test mode of the electronic circuit, the test unit comprising a combinatorial circuit having a plurality of inputs and an output, the combinatorial circuit implementing an exclusive logic function;

the I/O nodes being logically connected to the test unit in the test mode, wherein:

a first selection of the I/O nodes is arranged to carry respective input signals and is connected to the plurality of inputs of the combinatorial circuit;

a second selection of the I/O nodes comprises a first I/O node and is arranged to carry respective output signals, the first I/O node being coupled to the output of the combinatorial circuit;

the second selection of I/O nodes further comprises a second I/O node that is coupled to an I/O node from the first selection of I/O nodes in the test mode via a connection that bypasses the combinatorial circuit; and

at least one of the second I/O node is coupled to the I/O node from the first selection of I/O nodes via a buffer circuit and the third I/O node is coupled to the further I/O node from the first selection of I/O nodes via an inverter.

4. (Previously presented) The electronic circuit as claimed in claim 1, further comprising a test control node, the electronic circuit being arranged to switch to the test mode responsive to the reception of a test control signal on the test control node.

5. (Previously presented) The electronic circuit as claimed in claim 1, further comprising a main unit being logically connected to the I/O nodes in a functional mode of the electronic circuit, the main unit being arranged to bring the electronic circuit into the test mode upon receipt of a test control signal in a form of a predefined bit pattern through at least a subset of the first selection of I/O nodes.

6. (Previously presented) An electronic circuit arrangement, comprising:

an electronic circuit as claimed in claim 4 or 5; and

a further electronic circuit,

wherein the further electronic circuit is arranged to provide the electronic circuit with the test control signal and to provide the first selection of I/O nodes with test patterns for testing the electronic circuit.

7. (Previously presented) The electronic circuit arrangement as claimed in claim 6, wherein the further electronic circuit is arranged to receive test result data from the second selection of I/O nodes.

8. (Currently amended) A method for testing an electronic circuit, the electronic circuit comprising:

a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit;

a test unit for testing the electronic circuit in a test mode of the electronic circuit, the test unit comprising a combinatorial circuit having a plurality of inputs and an output, the combinatorial circuit implementing an exclusive logic function;

the I/O nodes being logically connected to the test unit in the test mode, wherein:

a first selection of the I/O nodes is arranged to carry respective input signals and is connected to the plurality of inputs of the combinatorial circuit; and

a second selection of the I/O nodes comprises a first I/O node and is arranged to carry respective output signals, the first I/O node being coupled to the output of the combinatorial circuit;

the method comprising the acts of:

logically connecting the test unit to the electronic circuit;

putting test data to the electronic circuit by the further electronic circuit; and

receiving test result data through the first I/O node;

receiving further test result data through a second I/O node from the second selection of I/O nodes, the second I/O node being coupled to an I/O node from the first selection of I/O nodes in the test mode via a connection that includes at least one of a buffer and an inverter, wherein the inverter facilitates a third I/O node from the second selection of I/O nodes being coupled to a further I/O node from the first selection of I/O nodes via a connection that bypasses the combinatorial circuit, and the buffer enables at least the second I/O node being coupled to the I/O node from the first selection of I/O nodes.